Amendments to the Drawing:

The gate 44 in Fig. 2 and the gate 114 in Fig. 3 are illustrated in wrong positions, and the amendments of drawings correct them.

Attachment:	Replacement Sheet	2 page(s)
	Annotated Sheet Showing Changes	2 page(s)

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REMARKS/ARGUMENTS

1. Amendment to the specification, claims 4, 12, 14, 20 and claims 1, 9:

The non-descriptive title has been written to describe more clearly the invention. The original title "CAPACITOR STRUCTURE" is now more descriptively prosed as, "STACKED CAPACITOR HAVING PARALLEL INTERDIGITIZED STRUCTURE FOR USE IN THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY".

Claim 20 is amended to correct spelling errors. Claims 4, 12, 14 are amended to delete the parenthetical limitations. No new matter is added.

Claim 1 is amended to add the limitation: the capacitor structure electrically connects to a thin film transistor (TFT) and the first conductive layer disconnects to a gate of the TFT in a display. The capacitor structure electrically connects to a thin film transistor is fully supported by paragraph [0024]: "The fifth conductive layer 138 extends to the thin film transistor area 105 to electrically connect the fourth conductive layer 132 to a drain 144 of the thin film transistor 108. In fact, the fifth conductive layer 138 is a signal line (not shown), and the fifth conductive layer 138 together with a scan line (not shown), electrically connected to the gate 114, are used to control the turn-on and turn-off of the thin film transistor 108." Besides, Fig. 3 supports the amendment of the first conductive layer disconnecting to a gate of the TFT in a display. Fig. 3 shows the first conductive layer 116 disconnects to the gate 114. No new matter is added in claim 1.

Claims 9, 11 are amended to correct the informality of referencing "a display" since **the display** is now previously mentioned in amended claim 1.

Claim 21 is added to mention: the gate and the capacitor are in the pixel array area. Claim 21 is supported by Fig. 3. Fig. 3 shows the gate 114 and the capacitor 112 are in the pixel array area 103. No new matter is added in claim 21.

2. Rejection of claims 1 and 3 under 35 U.S.C. 102 (b) as being anticipated by Burkhardt et al. (US 6,259,149).

Burkhardt et al. (US 6,259,149) is applied to the semiconductor, therefore the capacitor is in the trench 108 of the substrate 82. However, the applicant's invention is applied to the display; the capacitor 112 is not in any trench. Furthermore, the capacitor 112 of the applicant's invention connects to the TFT 108, but the capacitor of Burkhardt et al. doesn't connects to the TFT. The capacitor of Burkhardt et al. is fully isolated in the trench 108, and doesn't connect to the TFT. So, the capacitor of the applicant's invention is different from the capacitor of Burkhardt et al.. The amended claim 1 is patentably distinguishable from Burkhardt et al. (US 6,259,149). Reconsideration of the amended claim is politely requested.

The amended claim 1 is patentably distinguishable from Burkhardt et al. (US 6,259,149) for the above-mentioned reasons. The dependent claim 3 is also patentable.

3. Rejection of claims 1, 2, 4-17, 19-20 under 35 U.S.C. 102 (b) as being anticipated by Ikeda et al. (US 5,182,661).

The third storage capacitor electrode 68 of Ikeda et al. (US 5,182,661) cannot be regarded as similar to the first conductive layer 116 of the applicant's invention. The gate bus line 10 and the third storage capacitor electrode 68 (the first conductive layer) of Ikeda et al. are the same metal layer (Col 5, lines 58-60, "a third storage capacitor electrode 68 formed of chromium is provided to extend from of chromium is provided to extend from the gate bus line 10"). But, the first conductive layer 116 and the gate 114 of the applicant's invention are not the same metal layer as Fig. 3 shows. That causes the capacitor of Ikeda et al connects to the gate in the next pixel. But the capacitor 112 and the gate 114 of the applicant's invention are in the same pixel array area 103. The capacitor of the applicant's invention is different form the capacitor of Ikeda et al. (US 5,182,661). The amended claim 1 is patentably distinguishable from Ikeda et al. (US 5,182,661). Reconsideration of the amended claim is politely requested.

The amended claim 1 is patentably distinguishable from Ikeda et al. (US 5,182,661) for the above-mentioned reasons. The dependent claims 2, 4-17, 19-20 are also patentable.

4. Rejection of claims 18 under 35 U.S.C. 103 (a) as being anticipated by Ikeda et al. (US 5,182,661).

The amended claim 1 is patentably distinguishable from Ikeda et al. (US 5,182,661) for the above-mentioned reasons. The dependent claim 18 is also patentable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: Oct. 31, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Annotated Sheet Showing Changes

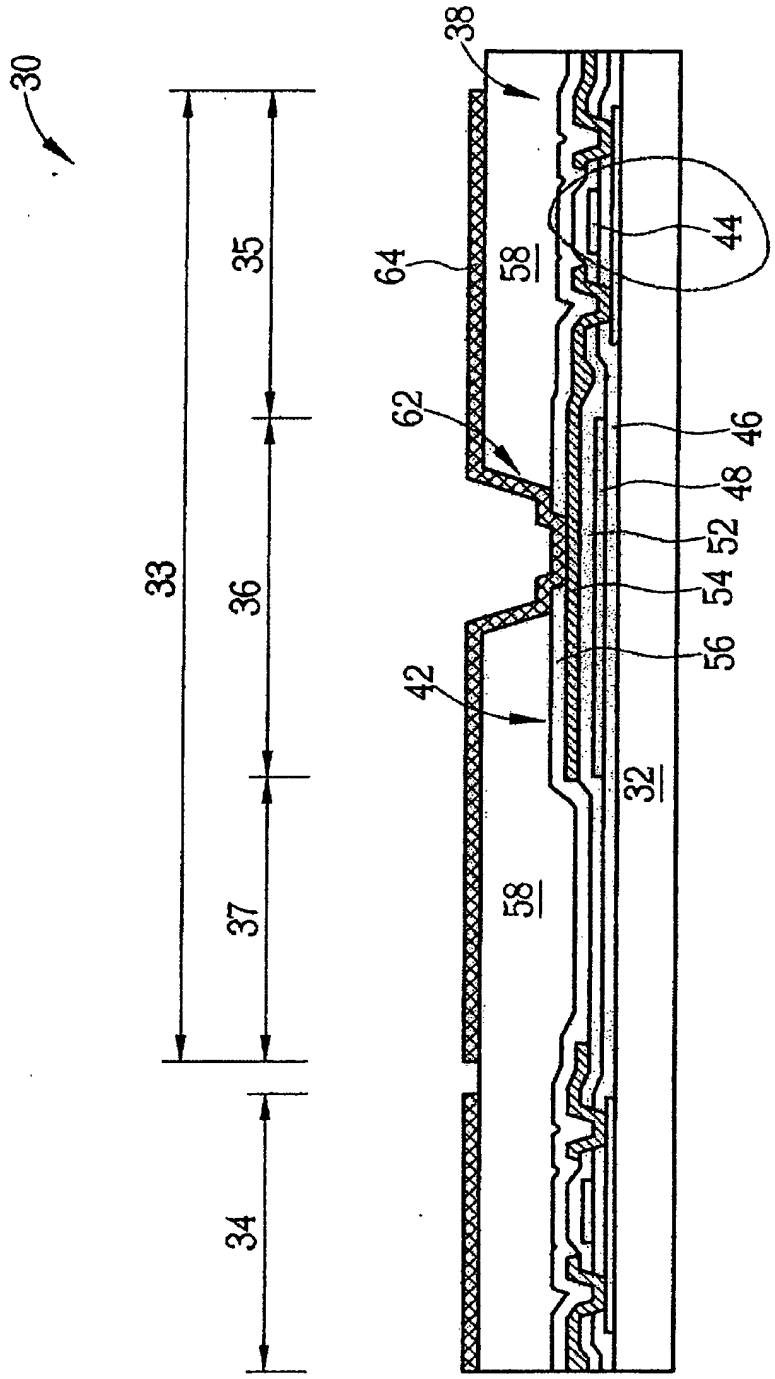

Fig. 2 Prior art

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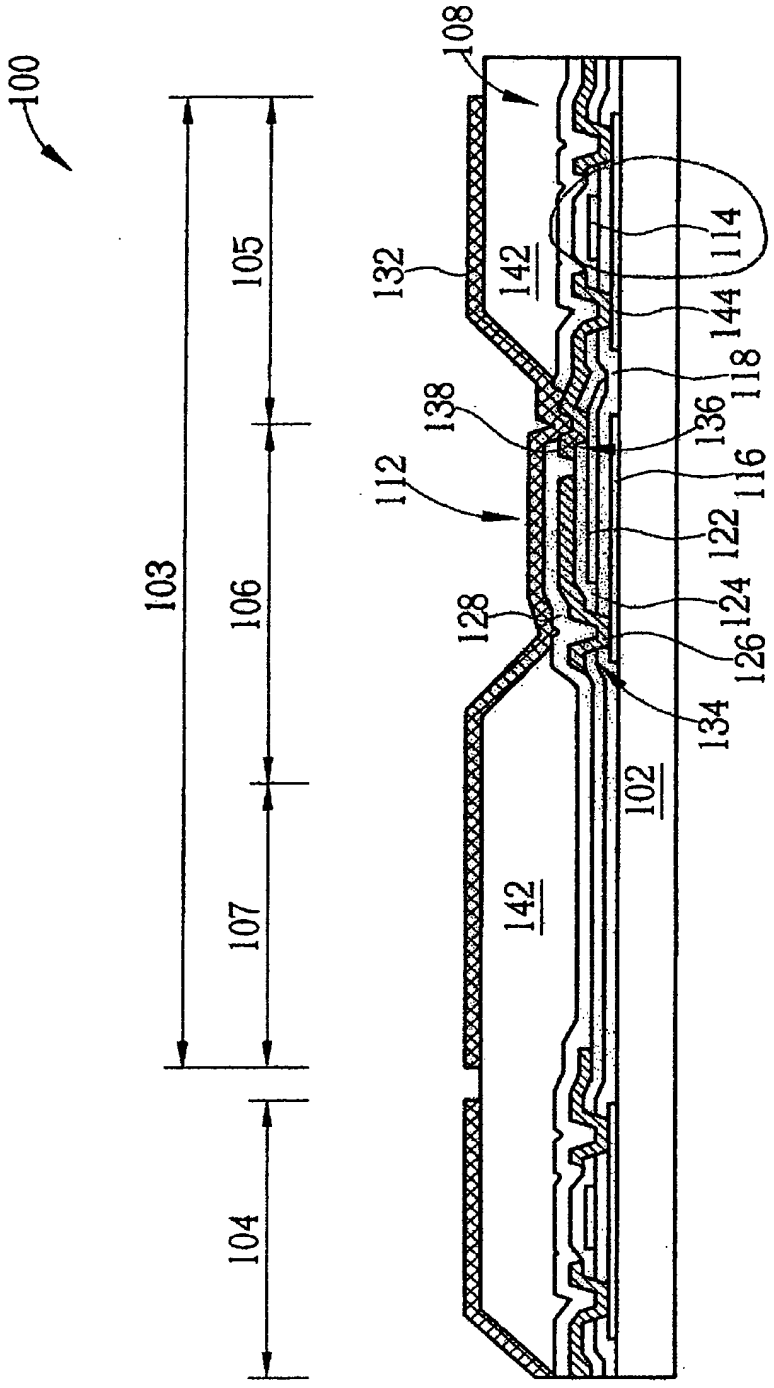

Fig. 3